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the compileultra command consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileultra at the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints. DC considers two RTL-to-Gates Synthesis using Synopsys Design Compiler

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CS250 Tutorial 5 (Version 091210b) September 12, 2010 Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

RTL-to-Gates Synthesis using Synopsys Design Compiler

The following command tells # the tool that the pin named clk is the clock and that the desired clock # period is 1 nanosecond. `dc_shell-topo> create_clock clk -name ideal_clock1 -period 1 #` The `compile_ultra` command begins the actual synthesis process that # transforms your design into a gate-level netlist.

RTL-to-Gates Synthesis using Synopsys Design Compiler

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